UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,911	09/28/2000	Sherry Solden	21891.03200	7789

7590 07/21/2004	EXAMINER
John W Carpenter	CRAIG, DWIN M
Crosby Heafey Roach & May	

ART UNIT	PAPER NUMBER
2123	

John W Carpenter
Crosby Heafey Roach & May
P O Box 7936
San Francisco, CA 94120-7936

DATE MAILED: 07/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/670,911	SOLDEN ET AL.
	Examiner	Art Unit
	Dwin M Craig	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>9-28-2000</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>28 September 2000</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
        application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date <u>4</u>.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-28 have been presented for Examination. Claims 1-28 have been Examined and

rejected.

Drawings

2.   The drawings filed on 9-28-2000 are acceptable subject to correction of the informalities;

specifically, figure 6 contains some hand written item numbers that need to be corrected. The

Drawings are suitable for examination however; formal drawings will be required when the case

is allowed.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3.   **Claim 4** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing

to particularly point out and distinctly claim the subject matter which applicant regards as the

invention.

It is unclear to the Examiner exactly what the *"other service declarations"* are referring

to and in what way these *"other service declarations"* are different.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4.   **Claims 1-3, 6-11, 12-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over

Pauna U.S. Patent 6,052,524 in view of **Testa et al. U.S. Patent 6,205,407.**

4.1   As regards independent **Claims 1 and 17** the *Pauna* reference discloses a method

of modeling an electronic system having both hardware and software elements **(Col. 4 Lines 30-**

33), capturing a plurality of behaviors that correspond to operations performed by the system

being modeled **(Col. 5 Lines 34-48),** *the Examiner notes that determining timing and behavior*

violations is functionally equivalent to capturing a plurality of behaviors, capturing a plurality of

hardware and software architectural components the plurality contained within an architectural

platform **(Col. 6 Lines 26-38),** mapping each of the captured behaviors of the plurality of

behaviors to a selected architectural component to perform the behavior **(Col. 8 Lines 26-45)**

and mapping each of the captured behaviors of the plurality of behaviors to a selected

architectural component to perform the behavior; **(Figure 3A Item 46, Figure 4A Item 70, Col.**

13 Lines 59-67, Col. 14 Lines 1-8), recognizing and capturing communications patterns **(Col. 4**

Lines 57-67, Col. 5 Lines 1-3, Table 7 Col. 12, Col. 12 Lines 64-67 Col. 13 Lines 1-4), *the*

Examiner notes that the memory read routines simulated using the pseudo-code listed in Table 7

are functionally equivalent to recognizing and capturing communications patterns, specifically

and in this case, the communications pattern of a processor reading from memory, among the

architectural components that require communication among them to perform the behaviors

(Figure 2 Items 22 and 24, 26 and 34), *the Examiner notes that the Pauna reference is directed*

towards the cycle accurate simulation of the communications between different components in a

system on a chip or SOC **(Col. 3 Lines 20-34).**

However, the *Pauna* reference does not clearly disclose, *mapping each instance of*

communications between behaviors <u>to an instance of the capture pattern.</u>

An artisan of ordinary skill, in the SOC simulation art, would have known that in order to

test the memory component in an SOC design, that certain test patterns would have to be

generated and verified in order to determine if the simulated memory component was *behaving*

properly. In the related art of testing ASICs, the *Testa et al.* reference discloses *mapping each*

instance of communications between behaviors <u>to an instance of the capture pattern</u> **(Cfigure 5**

Items 67, 64, all of Figures 6 & 7, Col. 7 Lines 30-52, Col. 12 Lines 5-14).

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the

invention was made, to have combined the component modeling methods of the *Pauna* reference

with the test pattern generation methods of the *Testa et al.* reference because, in order to properly

simulate and test an SOC design there is a need to generate and verify test pattern data that

simulates the interaction between the components in the SOC being designed in order to verify

that these components will interact correctly in the final design *(**Testa et al. Col. 2 Lines 28-33).**

4.2 As regards dependent **Claims 2 and 18** the *Pauna* reference discloses components having a plurality of services corresponding to a particular function of the hardware component **(Col. 3 Lines 35-49, Col. 4 Lines 50-67, Col. 5 Lines 1-3).**

4.3 As regards dependent **Claims 3** the *Pauna* reference discloses and API **(Col. 5 Lines 4-13).**

4.4 As regards dependent **Claims 6 and 22** the *Pauna* reference discloses hardware and software **(Col. 4 Lines 30-33).**

4.5 As regards dependent **Claim 7** the *Pauna* reference discloses a plurality of services, *API* **(Col. 5 Lines 4-13).**

4.6 As regards dependent **Claims 8, 9, 10, 12, 24, 25 and 26** the *Pauna* reference does not expressly discloses a history of test patterns **(Col. 8 Lines 26-45).**

4.7 As regards dependent **Claims 13 and 14** the *Pauna* reference discloses reuse of models **(Col. 4 Lines 57-67 Col. 5 Lines 1-3, Col. 8 Lines 26-45).**

4.8 As regards dependent **Claims 15, 16 and 23** the *Pauna* reference discloses a method for adding new architectures and changing the existing design from a library of components **(Col. 18 Lines 61-67 Col. 19 Lines 1-17).**

5. Independent **Claim 27** and dependent **Claims 5, 11 and 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Pauna U.S. Patent 6,052,524** in view of **Testa et al. U.S. Patent 6,205,407** and in further view of **Hill et al. U.S. Patent 6,438,514.**

5.1 As regards the rejections of Independent **Claims 1 and 17,** *from which dependent Claims 5 and 11 depend,* please see paragraph **4.1** above.

5.2   As regards Independent **Claim 27** the *Pauna* reference discloses an API **(Col. 5**

Lines 4-13), and a plurality of hardware and software architectural components the plurality

contained within an architectural platform **(Col. 6 Lines 26-38)**, mapping each of the captured

behaviors of the plurality of behaviors to a selected architectural component to perform the

behavior **(Col. 8 Lines 26-45)** and mapping each of the captured behaviors of the plurality of

behaviors to a selected architectural component to perform the behavior; **(Figure 3A Item 46,**

Figure 4A Item 70, Col. 13 Lines 59-67, Col. 14 Lines 1-8), recognizing and capturing

communications patterns **(Col. 4 Lines 57-67, Col. 5 Lines 1-3, Table 7 Col. 12, Col. 12 Lines**

64-67 Col. 13 Lines 1-4), *the Examiner notes that the memory read routines simulated using the*

pseudo-code listed in Table 7 are functionally equivalent to recognizing and capturing

communications patterns, specifically and in this case, the communications pattern of a

processor reading from memory, among the architectural components that require

communication among them to perform the behaviors **(Figure 2 Items 22 and 24, 26 and 34)**,

the Examiner notes that the Pauna reference is directed towards the cycle accurate simulation of

the communications between different components in a system on a chip or SOC **(Col. 3 Lines**

20-34).

However, the *Pauna* reference does not clearly disclose, *the first service being among a*

plurality of service supported by the pattern to which communication is mapped, and a

performance model of a component.

An artisan of ordinary skill, in the SOC simulation art, would have known that in order to

test the memory component in an SOC design, that certain test patterns would have to be

generated and verified in order to determine if the simulated memory component was *behaving*

properly. In the related art of testing ASICs, the *Testa et al.* reference discloses *mapping each instance of communications between behaviors to an instance of the capture pattern* **(Cfigure 5 Items 67, 64, all of Figures 6 & 7, Col. 7 Lines 30-52, Col. 12 Lines 5-14).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the component modeling methods of the *Pauna* reference with the test pattern generation methods of the *Testa et al.* reference because, in order to properly simulate and test an SOC design there is a need to generate and verify test pattern data that simulates the interaction between the components in the SOC being designed in order to verify that these components will interact correctly in the final design **(*Testa et al.* Col. 2 Lines 28-33).**

Hill et al. discloses a performance model **(Col. 2 Lines 40-60).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to provide a performance model of a component because by doing so comparison of different combinations of components could be performed without the high cost of actually fabricating the SOC **(Hill et al. Col. 2 Lines 61-64)**.

5.3   As regards dependent **Claim 28** the *Pauna* reference discloses three or more components **(Figure 2 Items 22, 24, 26, 34, 30 & 32)** and it would be obvious that each of these components would have multiple services to reflect their full functionality.

5.4   As regards dependent **Claims 5 and 11** the *Pauna* reference does not expressly disclose a performance model.

The *Hill et al.* reference discloses a performance model **(Col. 2 Lines 40-60).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to provide a performance model of a component because by doing so

comparison of different combinations of components could be performed without the high cost

of actually fabricating the SOC **(Hill et al. Col. 2 Lines 61-64)**.

Conclusion

6.   Claims 1-28 have been presented for Examination. Claims 1-28 have been Examined and

rejected. This Office Action is **NON-FINAL.**

6.1   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The

examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC